PRESENT CLAIMS

1. (Original) A method of fabricating a vertically integrated circuit, the method comprising the steps of:

providing a bulk substrate;

selectively creating strong bond regions and weak bond regions on said substrate;

providing a first bonded semiconductor layer vertically supported on said substrate;

creating semiconductor device portions on said first bonded semiconductor layer, said semiconductor device portions corresponding to said weak bond regions;

removing said first semiconductor layer from said bulk substrate; and

bonding said first semiconductor layer to a second semiconductor layer.

2. (Original) The method of claim 1 further comprising the step of aligning said first semiconductor layer with said second semiconductor layer having similarly positioned semiconductor device portions.

3. (Original) The method of claim 2, wherein said aligning step is mechanical alignment.

4. (Original) The method of claim 2, wherein said aligning step is optical alignment.

5. (Original) The method of claim 1 further comprising the step of creating semiconductor device portions on said second semiconductor layer.

6. (Original) The method of claim 5, wherein said second semiconductor layer has semiconductor device portions on said weak bond regions.

7. (Original) The method of claim 1, wherein the ratio of areas of said strong bond regions to said weak bond regions is greater than 1.

8. (Original) The method of claim 1, wherein the ratio of bond strengths of said strong bond regions to said weak bond regions is greater than 1.

9. (Original) The method of clam 1 further comprising the step of interconnecting said first semiconductor layer with said second semiconductor layer.

10. (Original) The method of claim 9, wherein said step of interconnecting is implemented at the edge of said semiconductor layers.

11. (Original) The method of claim 10, wherein said step of interconnecting is electrically coupling.

12. (Original) The method of claim 10, wherein said step of interconnecting is optically coupling.

13. (Original) The method of claim 9, wherein said step of interconnecting is performed vertically through said semiconductor layers.

14. (Original) The method of claim 5, further comprising the steps of:

removing said second semiconductor layer from said bulk substrate; and

bonding said second semiconductor layer to said first semiconductor layer.

15. (Original) The method of claim 1, further comprising the steps of:

providing an Nth semiconductor layer vertically supported on said bulk substrate, said Nth semiconductor layer having strong bond regions and weak bond regions;

creating semiconductor device portions on said Nth semiconductor layer, said semiconductor device portions corresponding to said weak bond regions;

removing said Nth semiconductor layer from said bulk substrate; and

bonding said Nth semiconductor layer to an (N-1)th semiconductor layer.

16. (Original) The method of claim 15, wherein active semiconductor elements are formed from any two of said N semiconductor layers.

17. (Original) The method of claim 1, further comprising the step of:

dicing said bonded semiconductor layers to form one or more dies.

18. (Original) The method of claim 17, further comprising the step of:

interconnecting said bonded semiconductor layers after said dicing step.

19. (Original) The method of claim 18, further comprising the step of:

forming edge connectors on the boundary of said one or more dies.

20. (Original) The method of claim 19 wherein said edge connectors serve as diagnostic conductors to determine health of individual die layers.

21. (Original) The method of claim 1, wherein said bulk substrate includes a buried oxide layer.

22. (Original) The method of claim 21, wherein said buried oxide layer is formed by ion implantation.

23. (Withdrawn) A vertical integrated circuit comprising:

a bulk substrate on a wafer;

a first selectively bonded semiconductor layer vertically supported on said substrate, said bonded semiconductor layer containing weak bond regions and strong bond regions;

a second selectively bonded semiconductor layer vertically supported on said first selectively bonded semiconductor layer;

wherein a semiconductor device portion is created at or on said weak bond regions, and

wherein said semiconductor device portion vertically spans said first selectively bonded semiconductor layer and said second selectively bonded semiconductor layer.

24. (Withdrawn) A vertical integrated circuit formed on a die comprising:

a bulk substrate on a wafer;

a first selectively bonded semiconductor layer vertically supported on said substrate, said bonded semiconductor layer containing weak bond regions and strong bond regions;

a second selectively bonded semiconductor layer vertically supported on said first selectively bonded semiconductor layer;

wherein a semiconductor device portion is created at or on said weak bond regions;

wherein said semiconductor device portion vertically spans said first selectively bonded semiconductor layer and said second selectively bonded semiconductor layer, and

wherein said die is formed by dicing said bonded semiconductor layers.